REMARKS

Applicants respectfully request further examination and reconsideration in view of the above amendments. Claims 1-3, 5-9, 12, 13 and 18-20 remain pending in the case. Claims 1-3, 5-9, 12, 13 and 18-20 are rejected.

35 U.S.C. §103(a)

Claims 1-3, 5-9, 12, 13 and 18-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent 5,437,017 by Moore et al., hereinafter referred to as the "Moore" reference, in view of "IBM Technical Disclosure Bulletin, May 1994, Vol. 37, Issue 5, pages 249-250 hereinafter referred to as the "IBMTDB 37" reference. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 1-3, 5-9, 12, 13 and 18-20 are not unpatentable over Moore in view of IBMTDB 37 for the following rationale.

Applicants respectfully direct the Examiner to independent Claim 1 that recites that an embodiment of the present invention is directed to (emphasis added):

> A system for maintaining translation consistency in a computer which includes a host processor designed to execute instructions of a host instruction set and software for translating instructions from a target instruction set to instructions of the host instruction set comprising:
>
> hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction; and

software means responding to an indication that a memory address to be written stores a target instruction which has been translated to at least one host instruction for assuring that host instructions translated from the target instructions stored at the memory address will not be utilized once the memory address has been written.

Claims 7, 12 and 18 provide similar limitations. Claims 2, 3, 5 and 6 that depend from independent Claim 1, Claims 8 and 9 that depend from independent Claim 7, Claim 13 that depends from independent Claim 12, and Claims 19 and 20 that depend from independent Claim 18 provide further recitations of the features of the present invention.

Applicants respectfully assert that the combination of Moore and IBMTDB 37 does not teach, describe or suggest the embodiments of the present invention recited in Claim 1. For instance, Moore and the present invention are very different. Applicants understand Moore to teach a method and system for maintaining translation lookaside buffer (TLB) coherency in a multiprocessor data processing system. In particular, Moore teaches a multiprocessor system including TLBs for translating effective/virtual addresses into real addresses within a system memory.

Applicants respectfully assert that Moore does not teach, describe or suggest a system for maintaining translation consistency in a computer including "hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one

host instruction," as claimed (emphasis added). With reference to Figure 1 of Moore, a multi-processor data processing system 6 includes multiple processors 10, each processor 10 including a TLB 40. The TLB is used for translating effective or virtual addresses into real addresses within system memory 18. In particular, because each processor 10 accesses system memory 18, coherency between all TLBs 40 must be maintained (col. 4, lines 19-30).

Applicants understand that the TLBs as taught in Moore are used for maintaining address translations of a multi-processor system. In particular, Moore does not teach, describe or suggest translating instructions of a target instruction set into a host instruction set and maintaining coherency between these translation types, e.g., host and target instructions.

In contrast, the present invention provides a system for maintaining translation consistency in a computer including "hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction," as claimed (emphasis added). As described in the specification, target instructions are translated into host instructions that are stored in a memory data structure (e.g., translation buffer) (page 24, line 24 through page 25, line 1). Specifically, a translated host instruction may be stored in the memory.

Furthermore, the claimed invention is for "maintaining translation consistency in a computer system which includes a host processor." The translation is performed by code morphing software of a single processor (page 22, line 17 through page 24, line 14). By holding translated instructions, the translated instructions may be efficiently recalled without rerunning an extensive translation process each time the target instruction or group of instructions is executed (page 25, lines 1-12).

Moreover, the combination of Moore and IBMTDB 37 fails to teach or suggest the claimed embodiments because IBMTDB 37 does not overcome the shortcomings of Moore. IBMTDB 37, either alone or in combination with Moore, does not show or suggest the invention as claimed. Applicants understand IBMTDB 37 to teach the use of the SYNC instruction to synchronize completion of TLB invalidate across processors in a multi-processor system.

Applicants respectfully assert that IBMTDB 37 does not teach, describe or suggest a system for maintaining translation consistency in a computer including "hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction," as claimed (emphasis added). As described above with reference to Moore, Applicants understand the TLB of IBMTDB 37 to store translated addresses for use in a multi-processor system. In particular,

IBMTDB 37 does not teach, describe or suggest translating instructions of a target instruction set into a host instruction set.

In contrast, as described in the current specification and claimed, the present invention provides that target instructions are translated into host instructions that are stored in a memory data structure.

Furthermore, the claimed invention provides for maintaining coherency because a write to one memory address containing an instruction prevents the associated translated version of the instruction from being invalid (are therefore usable). So, the combination also fails to teach the claimed "software means ... for assuring that host instructions translated from the target instructions stored at the memory address will not be utilized once the memory address has been written." This limitation is not taught because the cited combination fails to teach or suggest this type of translation coherency.

Applicants respectfully assert that nowhere does the combination of Moore and IBMTDB 37 teach, disclose or suggest the present invention as recited in independent Claims 1, 7, 12 and 18, and that Claims 1, 7, 12 and 18 are thus in condition for allowance. Therefore, Applicants respectfully submit that the combination of Moore and IBMTDB 37 also does not teach or suggest the additional claimed features of the present invention as recited in Claims 2, 3, 5 and 6 that depend from independent Claim 1, Claims 8 and 9 that depend

from independent Claim 7, Claim 13 that depends from independent Claim 12, and Claims 19 and 20 that depend from independent Claim 18. Applicants respectfully submit that Claims 2, 3, 5, 6, 8, 9, 13, 19 and 20 overcome the rejection under 35 U.S.C. § 103(a) as these claims are dependent on an allowable base claim.

CONCLUSION

In light of the above remarks, Applicants respectfully request reconsideration of the rejected claims. Based on the arguments presented above, Applicants respectfully assert that Claims 1-3, 5-9, 12, 13 and 18-20 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,
WAGNER, MURABITO & HAO L.L.P.

Dated: 17 Feb, 2005

Matthew J. Blecher
Registration No. 46,558

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060